A1022

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Kok-Weng Loo
Application No.	:	Not yet available
Confirmation No.	:	Not yet available
Filed	:	Concurrently herewith
For	:	GATE-BODY CROSS-LINK CIRCUITRY FOR METAL-OXIDE-SEMICONDUCTOR TRANSISTOR CIRCUITS
Group Art Unit	:	
Examiner	:	

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98, applicants hereby bring the attention of the Examiner to the documents listed on the attached Form PTO-1449 (submitted in duplicate).

A copy of each listed document is enclosed herewith.

Respectfully submitted,

G. Victor Treyz 1/26/04

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PTO/SB/08b (08-03)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

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Application Number	
Filing Date	Herewith
First Named Inventor	Kok-Weng Loo
Art Unit	
Examiner Name	
Attorney Docket Number	A1022

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Andy Wei et al. "Design Methodology for Minimizing Hysteretic Vt -Variation in Partially-Depleted SOI CMOS" (c) 1997 IEEE in IEDM 97 pp. 411-414	
		"SOI Technology: IBM's Next Advance in Chip Design" IBM Corporation (undated)	
		Ghavam G. Shahidi et al. "Partially-Depleted SOI Technology for Digital Logic," 1999 IEEE International Solid-State Circuits Conference, IEEE 1999	
		Jean-Luc Pelloie, "SOI CMOS requires complex modeling http://www.eetimes.com/story/OEG20020923S0060 September 23, 2002, EETIMES	
		Vaughn Betz et al., "Circuit Design, Transistor Sizing and Wire Layout of FPGA Interconnect," IEEE Custom Integrated Circuits Conference, 1999 pp. 1-4	
		Koushik K. Das et al., "Circuit Style Comparison based on the Variable Voltage Transfer Characteristic and floating B Ratio Concept of Partially Depleted SOI" (undated) 9/17/02	
		"CMOS Devices and Reliability - SOD Devices & Circuits (Session 16)" IEDM 1997	
		Alan Joch "Silicon on Insulator", Computerworld 12/18/00	
		"Silicon On Insulator" Technology Article - Devient PC http://www.deviantpc.com/articles/SOI/index.shtml (4/03)	
		"SOI Circuit Design Concepts" pp 34, 35, and 196-209	

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Sheet 2 of 2

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Robert Richmond, "Silicon-on-Insulator Technology" www.sysopt.com/articles/soi/index3.html 11/8/00	
		"Silicon on Insulator"; http://www.okisemi.com/jp/english/bt-soi.htm 4/25/03	
		Jacques Gautier et al., "SOI Floating-Body, Device and Circuit Issues", IEDM 1997 pp 407-410	
		J.P. Colinge et al., "Potential of SOI for Analog and Mixed Analog-Digital Low-Power Applications, 1995 IEEE International Solid-State Circuits Conference (IEEE 1995)	
		Carlos Mazure et al., "ICs tailored for exotic substances", EE Times, 9/23/2002	
		Andre Auberton-Herve, "SOI sharpens the leading edge as silicon scales to 90 nanometers", EE Times 9/23/2002	

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